

LISTING OF CLAIMS

Claims 1-32. (Cancelled)

33. (Original) A method for operating a memory device including a single transistor formed on a substrate, wherein the single transistor is a memory transistor having a gate with a nonvolatile memory element, and the nonvolatile memory element is connected to a bit line comprised of first and second bit lines passing across the gate, wherein an addressing voltage and a write voltage are applied to the gate and the bit line, respectively, to write data to the nonvolatile memory element.

34. (Original) The method of claim 33, wherein first and second write voltages are applied to the first and second bit lines, respectively, to store data "1" and "0" to the nonvolatile memory element, and the first and second write voltages are the same as or different from each other.

35. (Original) The method of claim 33, wherein a second write voltage is applied to the first bit line to store data "1", a first write voltage is applied to the second bit line to store data "0", and the first and second write voltages are the same as or different from each other.

36. (Original) The method of claim 33, wherein a first write voltage is applied to the second bit line to store data, and a second write voltage higher than the first write voltage is applied to the second bit line to store different data.

37. (Original) The method of claim 33, wherein the written data is read by measuring the conductivity of the nonvolatile memory element.

38. (Original) The method of claim 37, wherein an addressing voltage is applied to the gate, and then a current measuring means is connected to the first bit line to measure current between the gate and the first bit line and thus the conductivity of the nonvolatile memory element.

39. (Original) The method of claim 38, wherein data "1" or data "0" is read depending on the measured current.

40. (Original) A method for operating a memory device including a substrate, a transistor formed on the substrate, the transistor having a gate, a drain connected to a bit line, and a source connected to a source of another transistor, a nonvolatile memory element formed between the gate and the substrate, and a metal line parallel to a word line connected to the transistor, wherein data is written by changing the conductivity of the nonvolatile memory element when the metal line is grounded.

41. (Original) The method of claim 40, wherein the nonvolatile memory element is comprised of a material layer for storing carriers, and semiconductor quantum dots formed thereon.

42. (Original) The method of claim 41, wherein a write voltage and an addressing voltage are applied to the bit line and the word line, respectively, when the metal line is grounded, to write data by changing the conductivity of the carrier storing material layer.

43. (Original) The method of claim 42, wherein data is written by changing the addressing voltage while the write voltage remains constant.

44. (Original) The method of claim 42, wherein data is written by changing the write voltage while the addressing voltage remains constant.

45. (Original) The method of claim 40, wherein the written data is read by measuring the conductivity of the nonvolatile memory element.

46. (Original) The method of claim 45, wherein a read voltage is applied to the bit line, and then a current measuring means is connected to the metal line to measure current

between the bit line and the metal line and thus the conductivity of the nonvolatile memory element.

47. (Original) The method of claim 46, wherein a different first or second read voltage is applied to the bit line to measure current between the bit line and the metal line and thus read data.

48. (Original) The method of claim 45, wherein a read voltage and an addressing voltage are applied to the metal line and the word line, respectively, and then a current measuring means is connected to the bit line to measure current between the metal line and the bit line and thus the conductivity of the nonvolatile memory element.

49. (Original) The method of claim 47, wherein data "0" is read when the measured current is large and the data "1" is read when the measured current is small.

50. (Original) The method of claim 48, wherein data "0" is read when the measured current is large and the data "1" is read when the measured current is small.

51. (Original) A method of manufacturing a memory device comprising:
defining a field region and an active region in a substrate;
forming a field oxide layer on the field region;
forming an insulating layer on the active region;
patterning the insulating layer to form first and second bit lines separated from and parallel to each other on the active region;
forming a memory element for storing data in a nonvolatile state on the insulating layer and the first and second bit lines so that the memory element passes across the first and second bit lines; and
forming a word line on the insulating layer and the memory element.

52. (Original) The method of claim 51, wherein the step of forming the memory element further comprises:
forming a plurality of spaced semiconductor quantum layers on the insulating layer and the first and second bit lines; and
forming an amorphous material layer covering the semiconductor quantum dots on the insulating layer.

53. (Original) The method of claim 51, wherein the step of forming the memory element comprises:
forming an amorphous material layer on the insulating layer and the first and second bit lines; and
forming spaced semiconductor quantum dots on the amorphous material layer.

54. (Original) The method of claim 52, wherein the amorphous material layer is an amorphous dielectric layer.

55. (Original) The method of claim 54, wherein the amorphous dielectric layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO₂).

56. (Original) The method of claim 53, wherein the amorphous material layer is an amorphous dielectric layer.

57. (Original) The method of claim 56, wherein the amorphous dielectric layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO₂).

58. (Original) The method of claim 52, wherein the semiconductor quantum dots are silicon dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage.

59. (Original) The method of claim 53, wherein the semiconductor quantum dots are silicon dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage.

60. (Original) A method of manufacturing a memory device, the method comprising:

forming a nonvolatile amorphous material layer on a substrate; and

forming a transistor on the nonvolatile amorphous material layer so that semiconductor quantum dots for emitting carriers to the amorphous material layer or recapturing the emitted carriers by application of a voltage are formed between the transistor and the amorphous material layer.

61. (Original) The method of claim 60, wherein the step of forming the transistor comprises:

forming first and second metal layer patterns on the nonvolatile amorphous material layer;

forming semiconductor quantum dots on the nonvolatile amorphous material layer between the first and second metal layer patterns;

forming a gate insulating layer covering the resultant in which the semiconductor quantum dots are formed on the substrate; and

forming a word line corresponding to the semiconductor quantum dots on the gate insulating layer.

62. (Original) The method of claim 60, wherein the nonvolatile amorphous material layer is formed of an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

63. (Original) The method of claim 60, wherein the semiconductor quantum dots are silicon dots.

64. (Original) The method of claim 61, further comprising:
forming an interlayer dielectric layer covering the word line on the gate insulating layer;
forming a via hole for exposing the first metal layer pattern; and
forming a fourth metal layer pattern for filling the via hole and passing across the word
line on the interlayer dielectric layer.